

The diagram illustrates the system architecture centered around the AMD APU and AMD FCH (Fusion Controller Hub). The APU is connected to the FCH via a UMI x 4 interface. The FCH manages various system components, including memory, storage, and I/O.

AMD APU Components:

- Processor:** RICHLAND Daul / Quad Core
- Power:** 25 (Watt)
- Package:** FP2 827-PIN BGA
- Size:** 27 x 31 (mm)

AMD FCH Components:

- Processor:** Bolton M3
- Power:** 4.7 Watt
- Package:** 656pin FCBGA
- Size:** 24.5 x 24.5 (mm)

Memory and Storage:

- DDR3 SODIMM1:** Maxima 8GBs (PAGE 11)
- DDR3 SO-DIMM2:** Maxima 8GBs (PAGE 12)
- VRAM:** DDR3 x 4 (900 MHz), 128 x 16 x 4, 64 bit, 256 x 16 x 4, 64 bit, Max 1GBs (PAGE 18)
- SATA - 1st HDD:** Package: 9.5 (mm), Power: (PAGE 24)
- SATA - ODD:** Power: (PAGE 24)

I/O and Peripherals:

- LAN:** RTL8166EH LAN CHIP, Power: (PAGE 22), Package: QFN32, Size: 4 x 4 (mm)
- WLAN / BT Combo:** Halt Mini Card, Power: (PAGE 26), Package: (PAGE 26), Size: (PAGE 26)
- USB:** USB 2.0/3.0 Combo x 2 (PAGE 25), USB 2.0 x 2 (PAGE 25)
- Camera:** (PAGE 20)
- External USB:** (PAGE 25)
- BT:** (PAGE 26)
- USB2.0 x 2:** (PAGE 25)
- HDMI Conn:** (PAGE 20)
- LCD Conn:** (PAGE 20)
- eDP:** (PAGE 20)
- DP Port2:** (PAGE 02-05)
- DP Port0:** (PAGE 19)
- RTD2132R:** DP to LVDS Translator (PAGE 19)

Other Components:

- System BIOS SPI ROM:** (PAGE 08)
- EC SPI ROM:** (PAGE 27)
- Keyboard:** (PAGE 25)
- Touch Pad:** (PAGE 24)
- SLG3NB242 GreenCLK:** (PAGE 26)
- FAN Controller:** (PAGE 24)
- Daughterl/B CONN Combo Jack:** (PAGE 21)
- Realtek RTS5239 Card Reader:** (PAGE 23)
- ALC3227-GR Audio Codec:** (PAGE 21)
- ITE IT8528E/HX Embedded Controller TOP:** (PAGE 27)

Interfaces and Connections:

- PCI-E Gen3 x 8 Lane:** Connects APU to FCH.
- PCI-E Gen1 x 1 Lane:** Connects FCH to various peripherals.
- SATA0 6GB/s:** Connects FCH to SATA drives.
- UMI x 4:** Connects APU to FCH.
- Green CLK 32.768KHz:** Connects FCH to various components.
- 25MHz:** Connects FCH to various components.

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

BQ24728
System Charge Power (+BATCHG)

G5934RZ1U
System Discharge Power
(+1.5V/+3V/+5V)
(+3VSUSV/+3VLAVCC/+1.1V)

Ricktek RT8223PZ
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

SL6277/RT8228AZ/AP3407A/ISL6208BCRZ
Processor Power (+VCC_CORE/
+1.2V/+2.5V/+VDDNB_CORE)

TPS51216RUKR

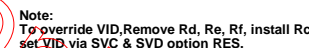
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

AOZ1237QI-02
PCH Power (+1.1VS5)

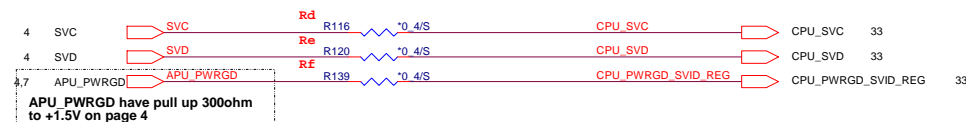
ADP3211A
DGPU Power (+VGA_CORE/+1.0V_VGA/+3V_VGA/
+1.5V_VGA/+1.8V_VGA/+VDDCI)



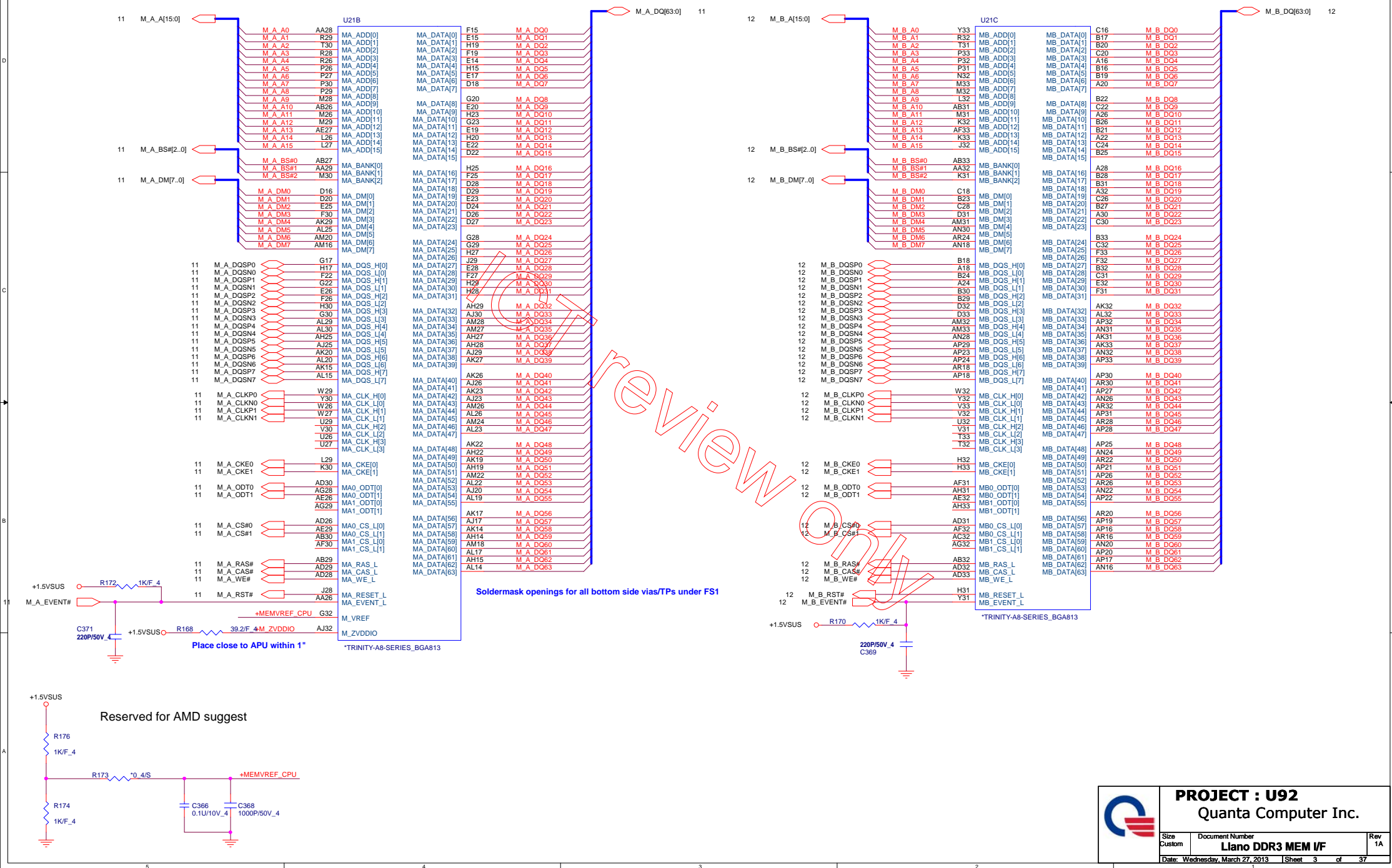
VID Override Circuit



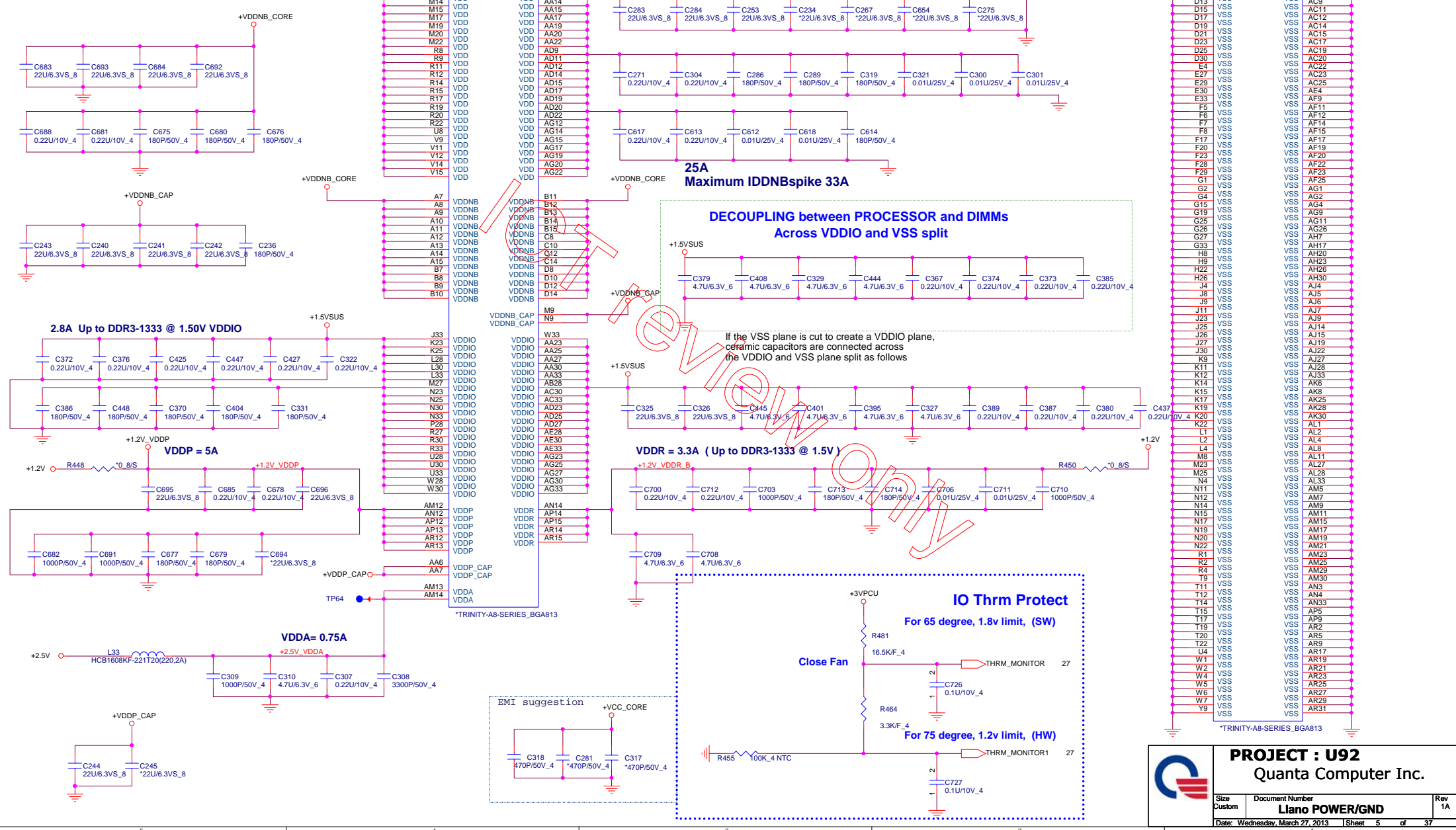
		BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8



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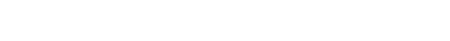
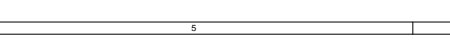
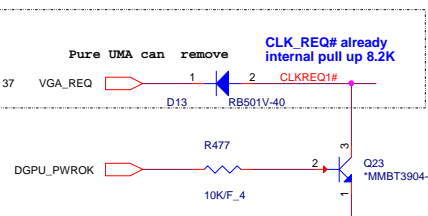
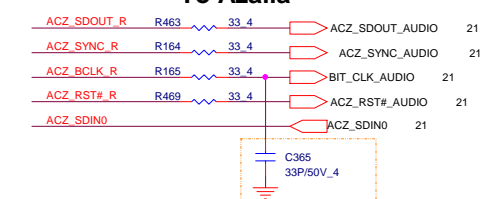
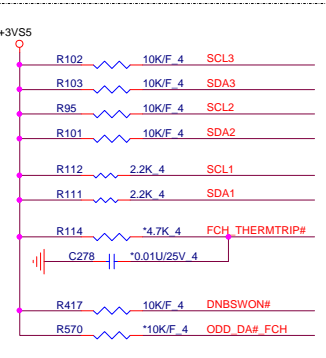
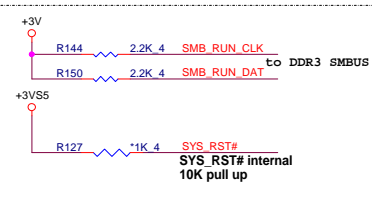
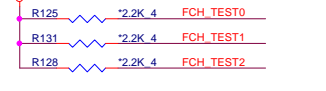


PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

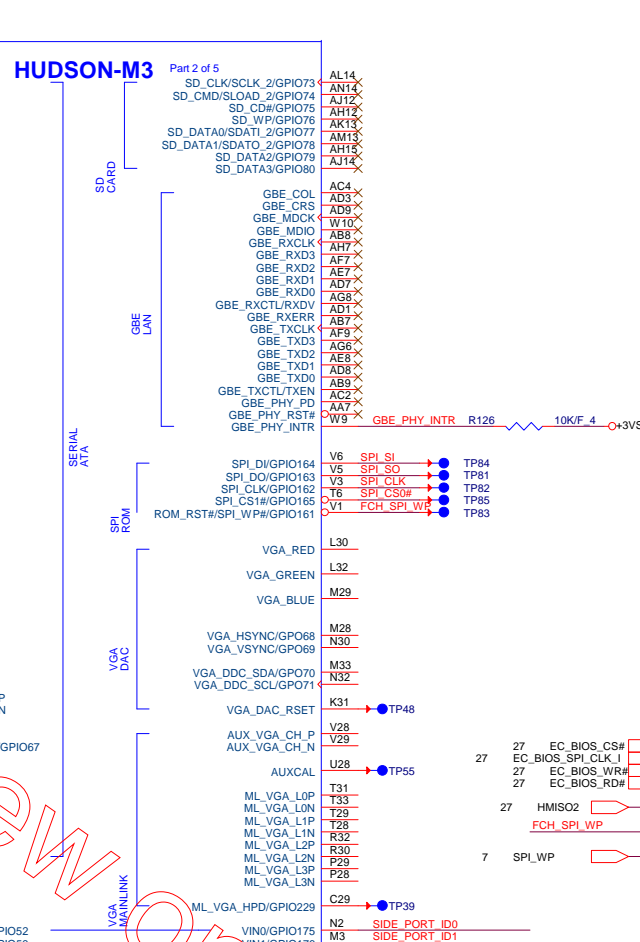
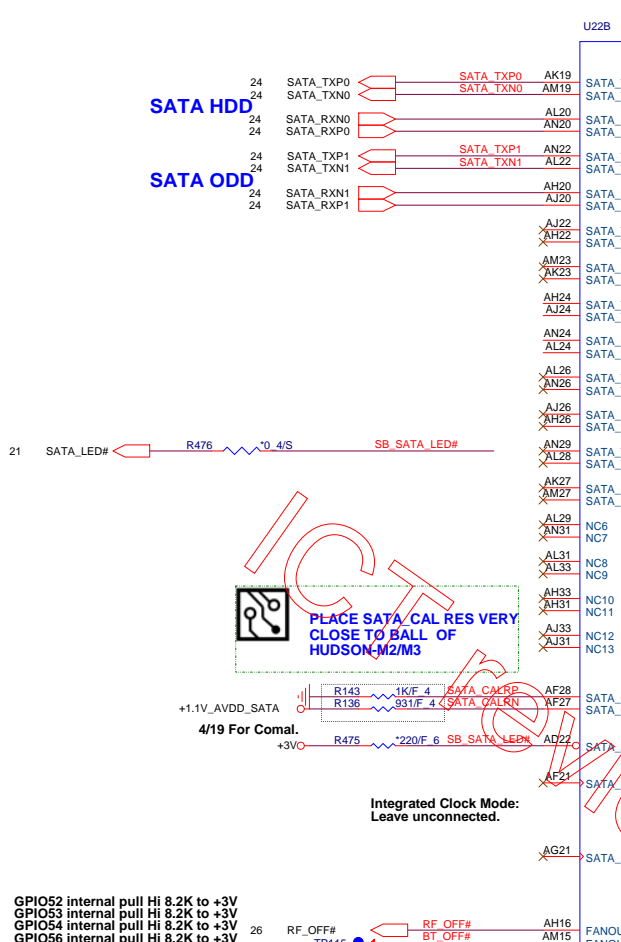
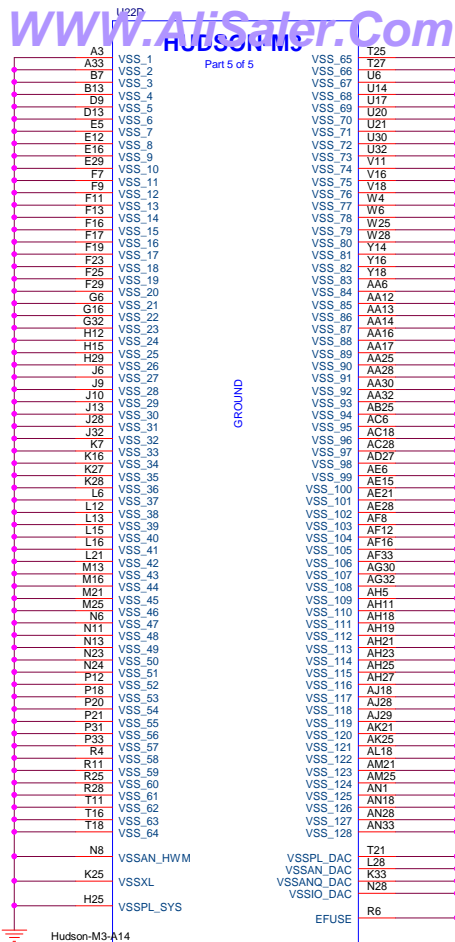


PROJECT : U92
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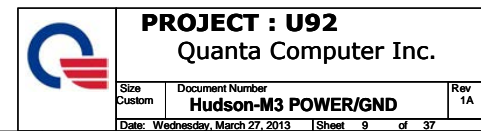
ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA 14"		1
0	0	0	1	0	UMA 15"		2
0	0	1	0	0	eDP panel		3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
0	0	0	0	1	SG / Muxless 14		9
0	0	0	1	1	SG / Muxless 15		10
1	0	0	1	1			11
1	0	1	1	1			12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no support side port

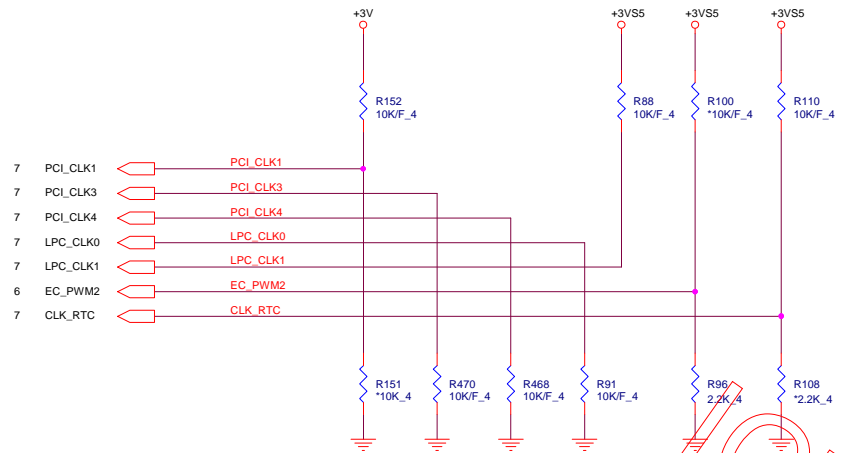
PROJECT : U92
Quanta Computer Inc.

Size Custom Document Number Hudson-M3 SATA/HWM/SPI Rev 1A

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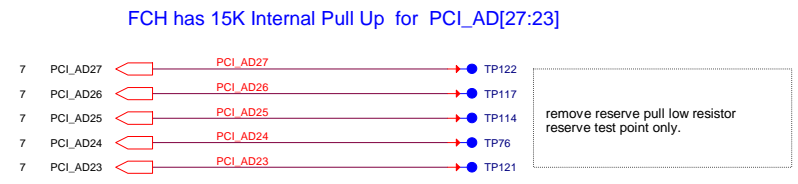
STRAP PINS
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

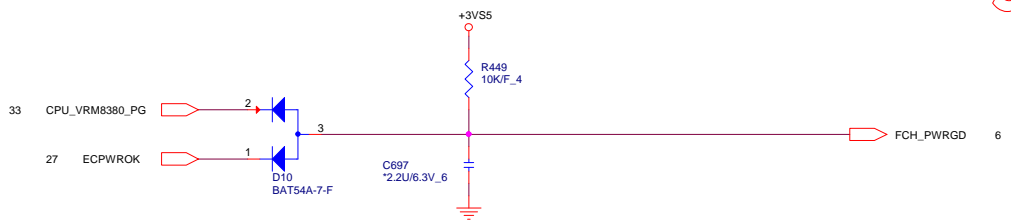
		PCI_CLK1		PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE ENABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE DISABLED

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH_PWRGD





Three circuit diagrams illustrating capacitor placement for DDR3 memory modules. The diagrams show the top and bottom of the module and internal circuitry.

Top of Module:

- +1.5VSUS:** C440, C418, C424, C439, C415, C412, C428, C438, C398, C442, C441, C449, C436.
- +0.75V_DDR_VTT:** C410, C413, C416, C419, C432, C435.
- +VREF_DQ0:** C393, C396 (Note: SI, change to 1000P to meet ref design).
- +VREF_CA0:** C431, C430, C429.

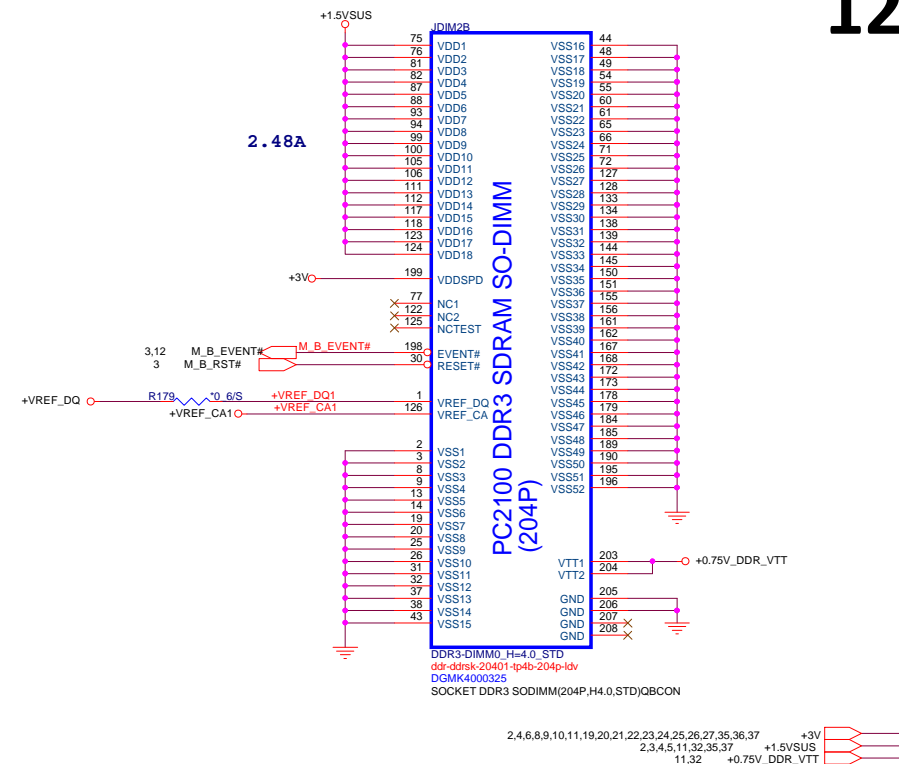
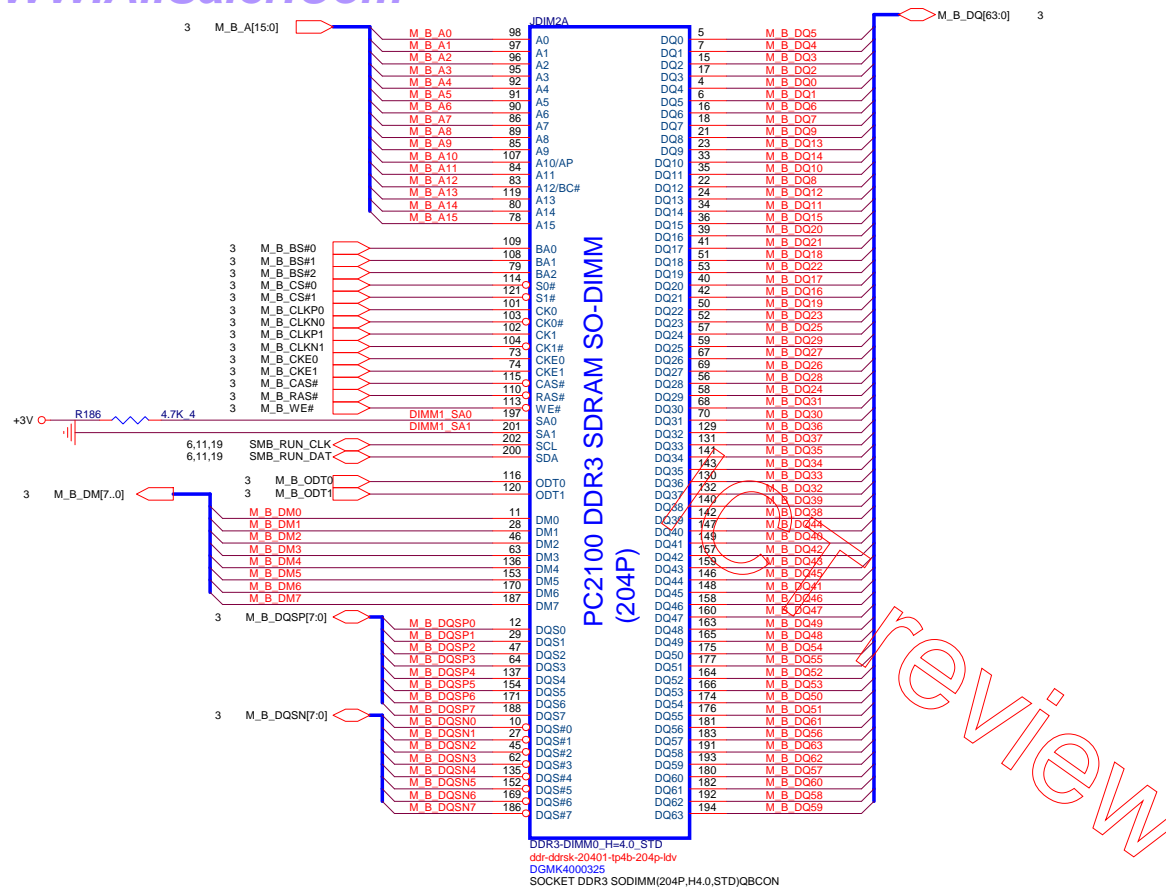
Bottom of Module:

- +1.5VSUS:** EC19, EC20, EC12, EC39, EC16, EC18, EC37, EC21.
- +0.75V_DDR_VTT:** EC34, EC33.

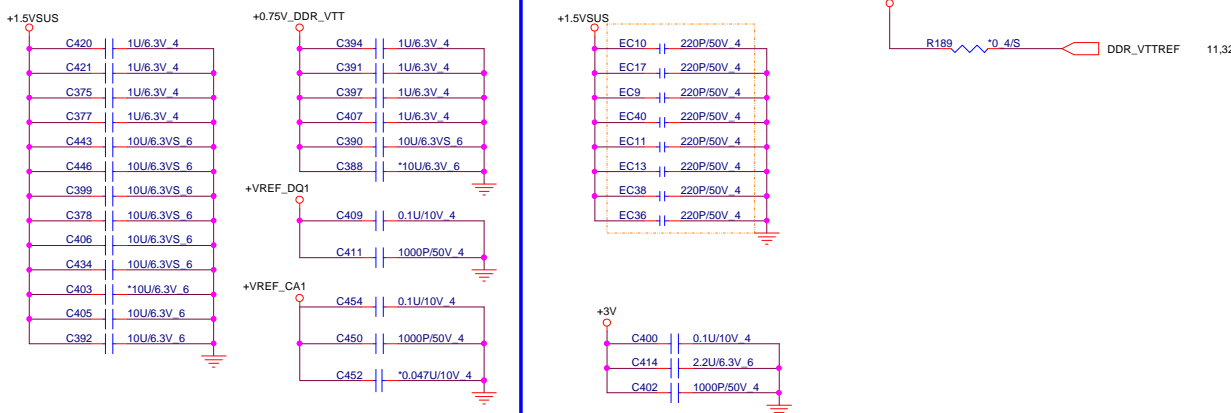
Internal Circuitry:

- +VREF_CA0:** R188, *0.4/S, DDR_VTTREF.

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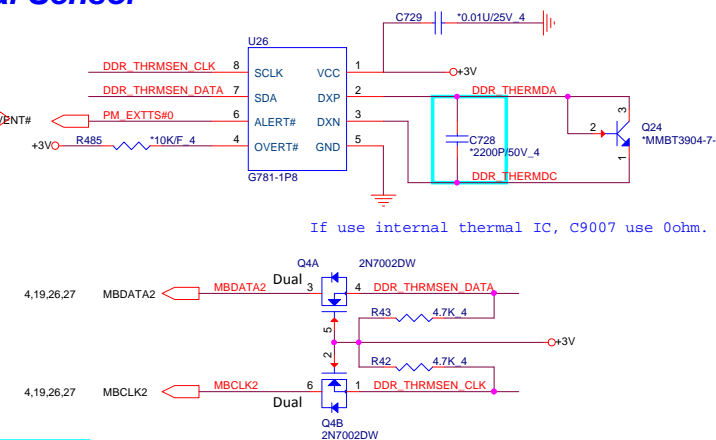


Place these Caps near So-Dimm1.



Local Thermal Sensor

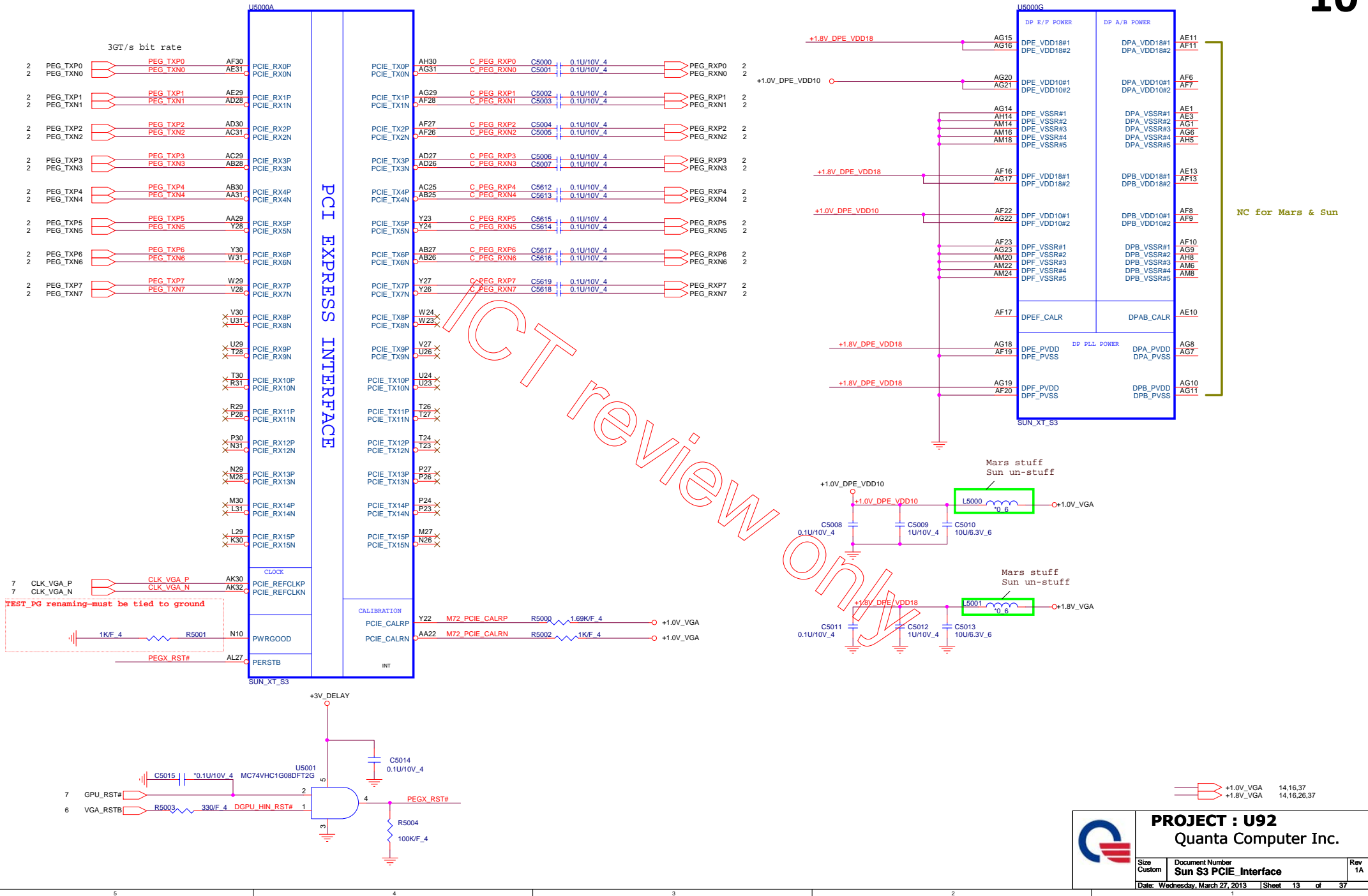
DDR3 Thermal Sensor



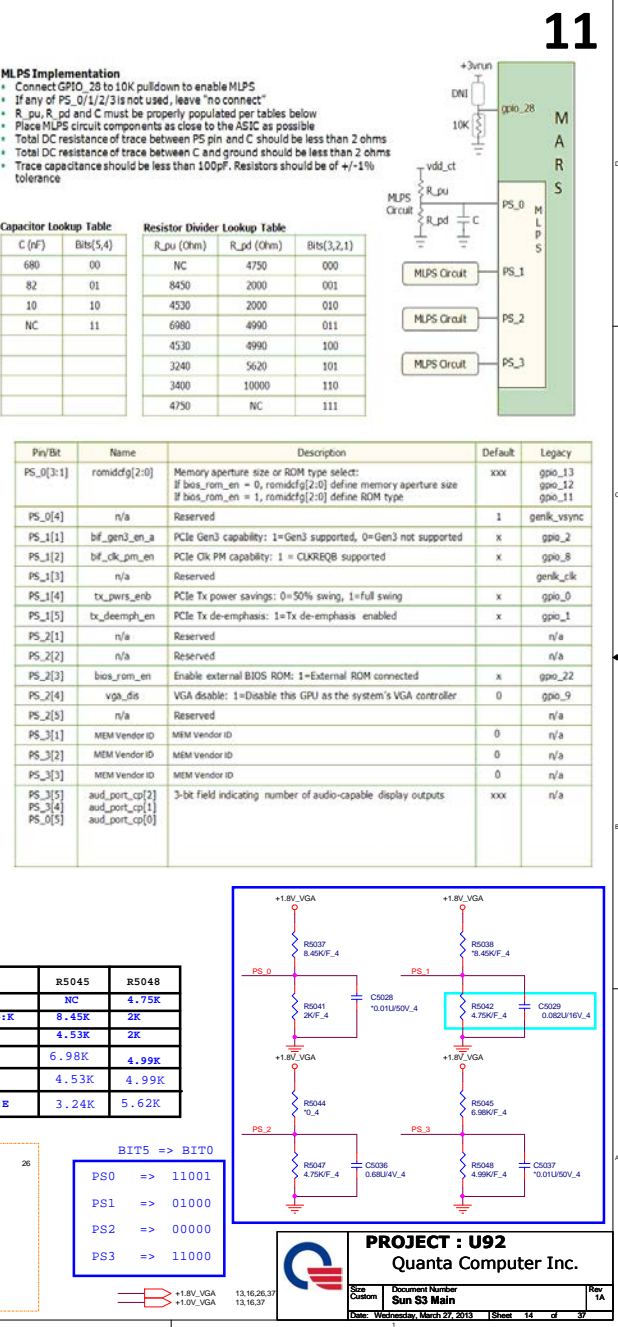
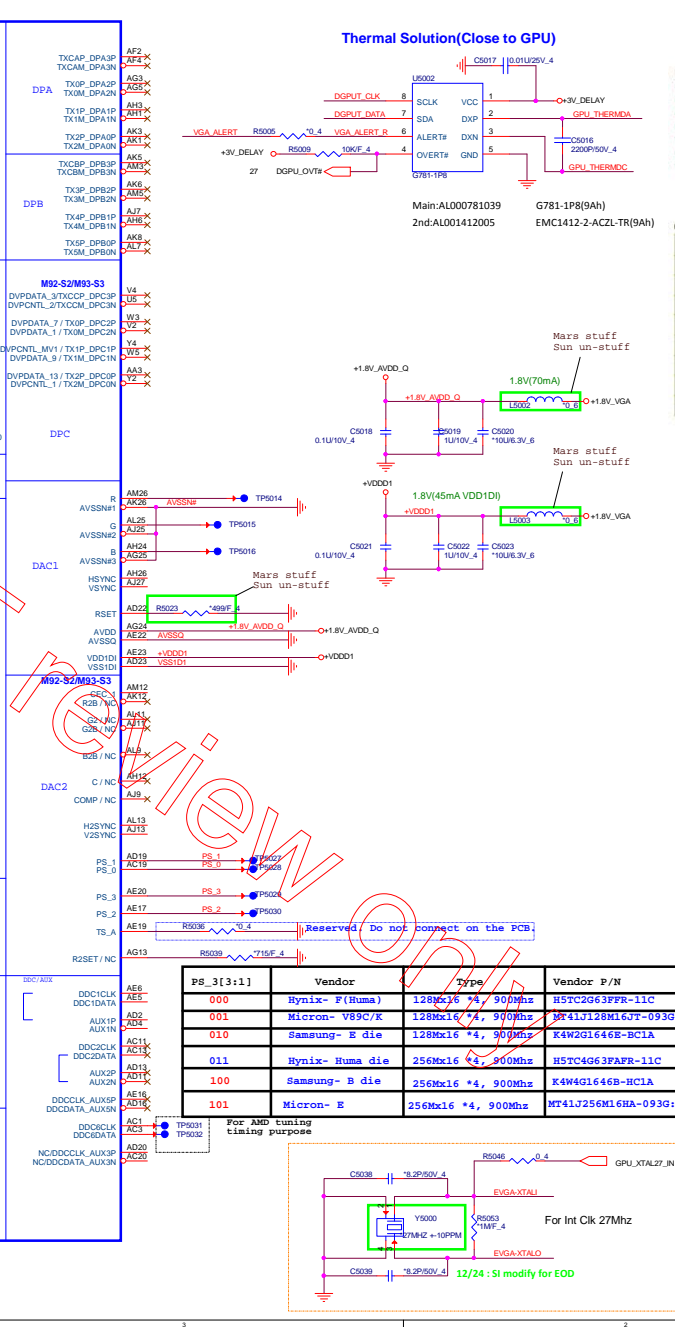
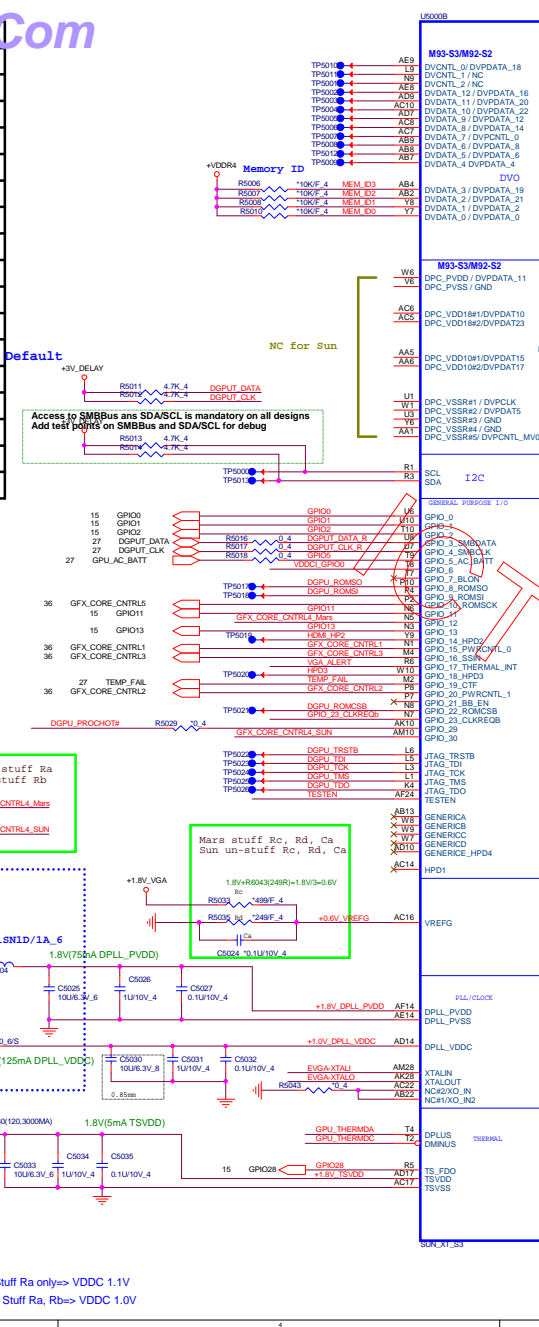
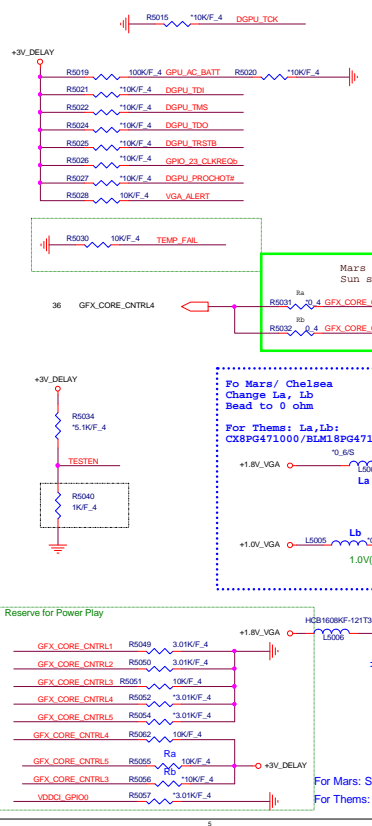
If use internal thermal IC, C9007 use 0ohm.

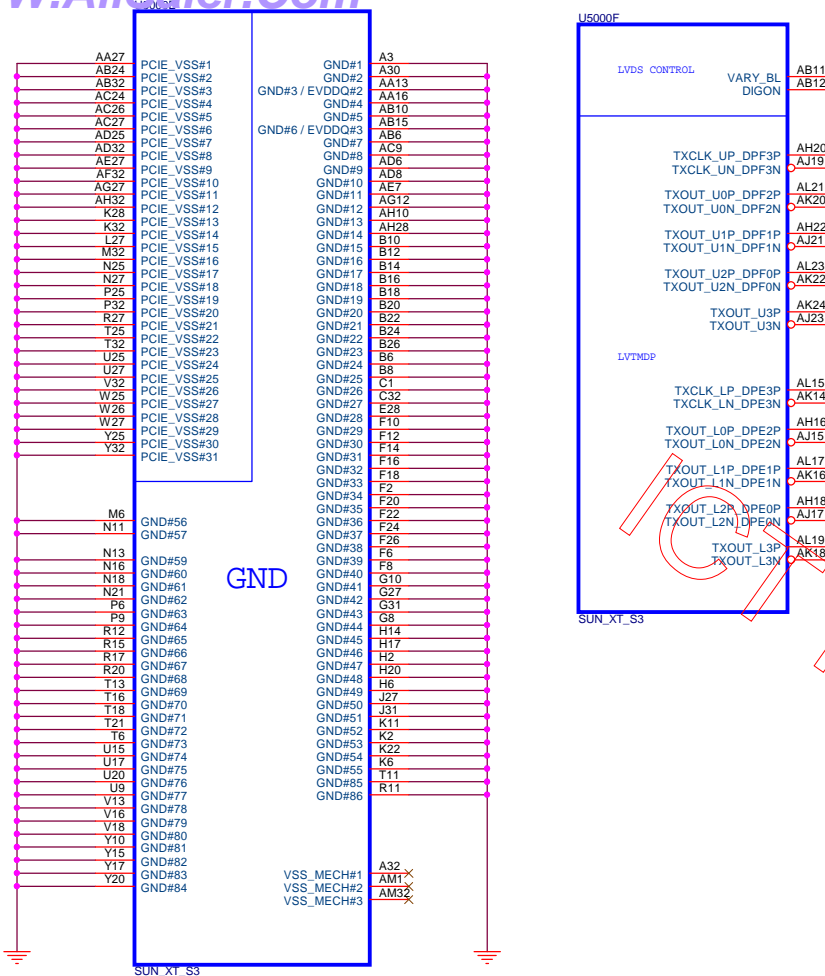
Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

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Size	Document Number	Rev
Custom	System Memory 2/2 (9.2H)	1A
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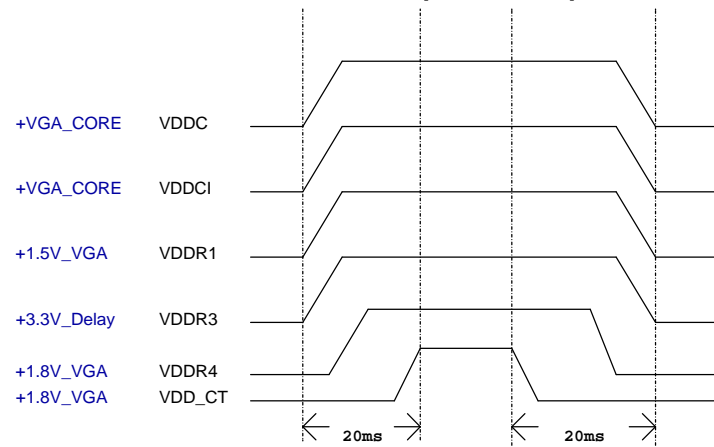


GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun S3
0	1	1	0	1	1.175V
0	1	1	1	1	1.150V
0	1	1	1	1	1.125V
1	0	0	0	1	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	1	0	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	1	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	1	0.850V
1	1	1	0	1	0.825V
1	1	1	1	0	0.800V
1	1	1	1	1	0.775V





Power Up/Down Sequence



Memory Aperture size(Seymour)

GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

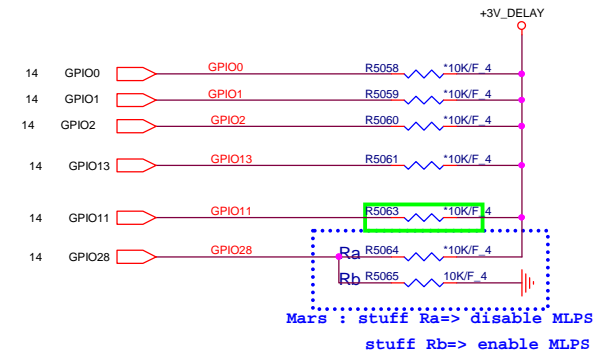
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIOQ[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUDI[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUDI[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

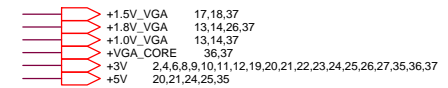


Mars : stuff Ra=> disable MLPS
stuff Rb=> enable MLPS



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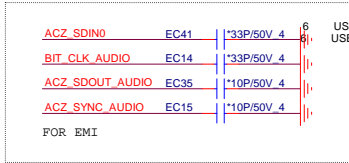
Size Custom	Document Number	Rev 1A
	Sun S3 GND / LVDS/ Straps	
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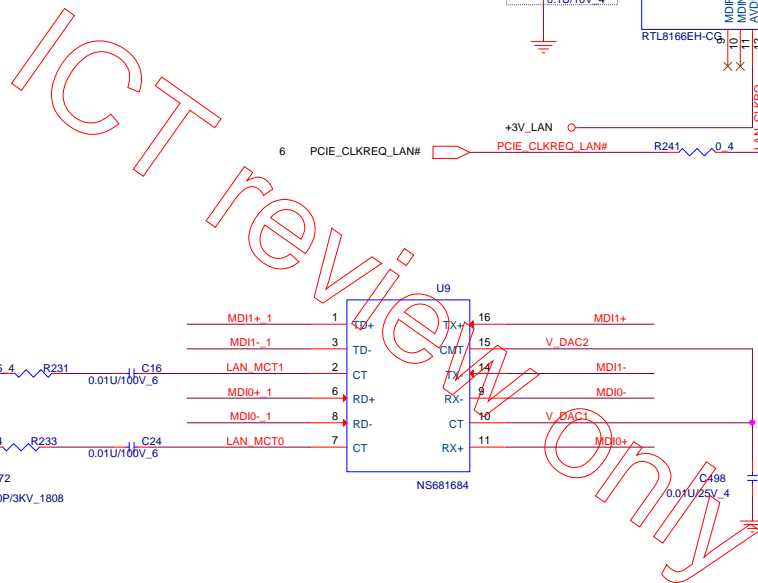


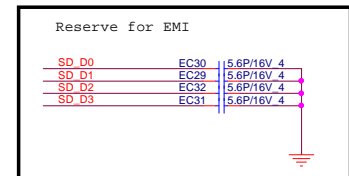
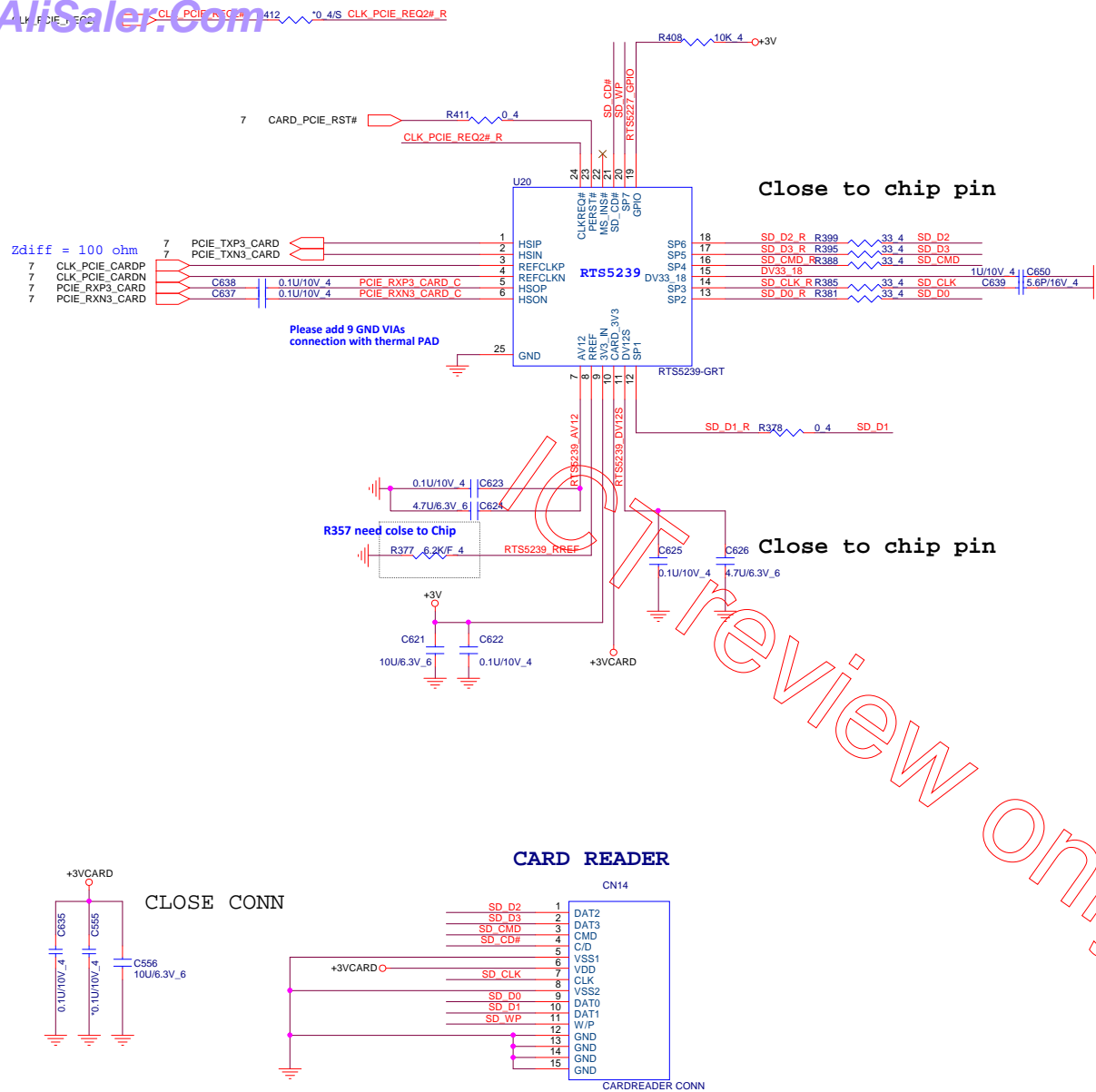




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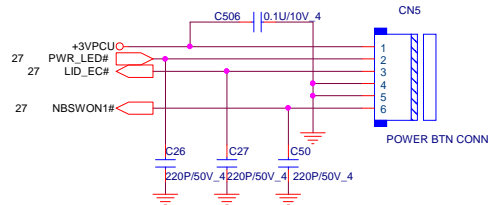




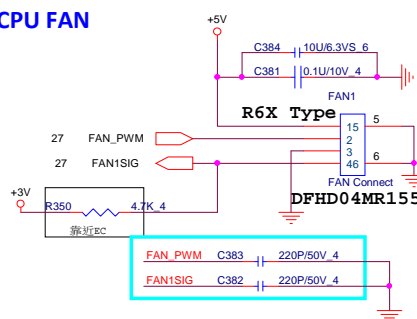


Power Button Connector

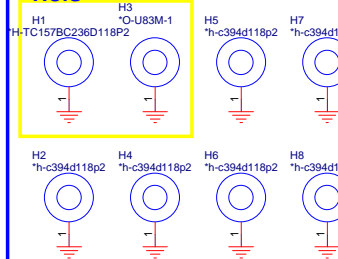
Pin1 : +3V (U15DSWITCH PWR)
Pin2 : PWR_LED#
Pin3 : LID_SWITCH#
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



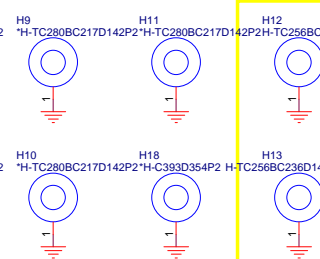
CPU FAN



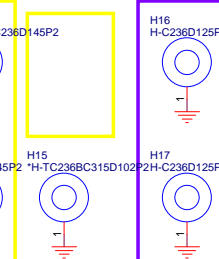
Hole SI change footprint



SI change FAN NUT P/N



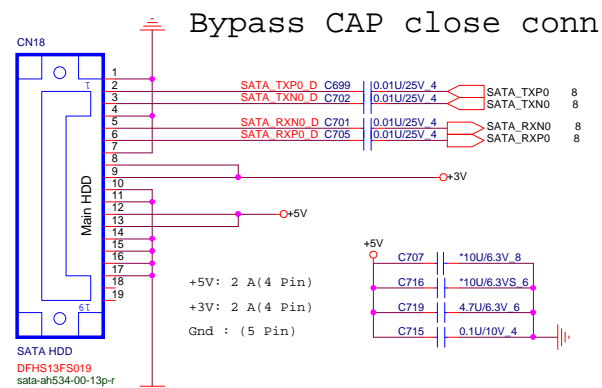
SI Del WLAN NUT



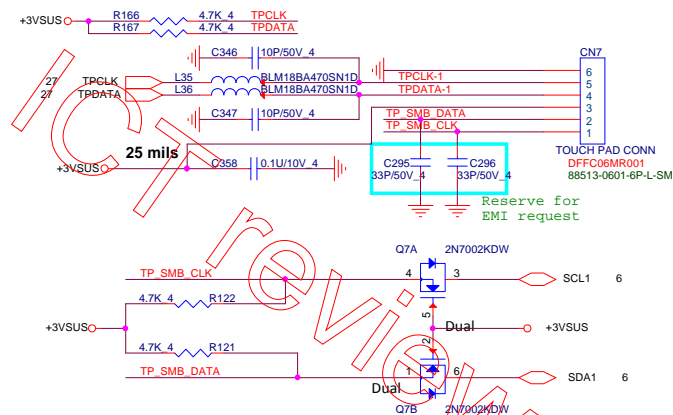
FAN NUT

PCH NUT

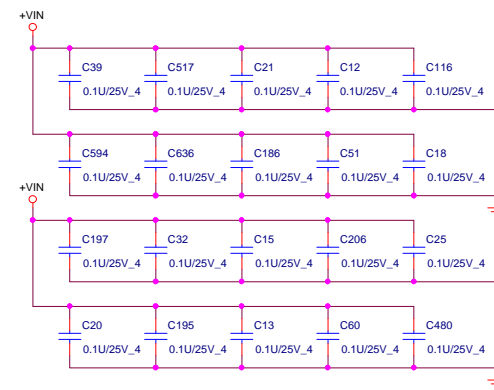
SATA HDD Connector(Cable type)



Touch Pad

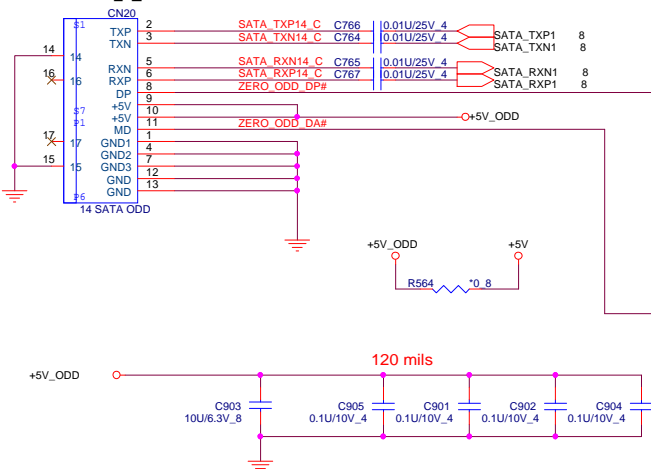


+VIN Cap

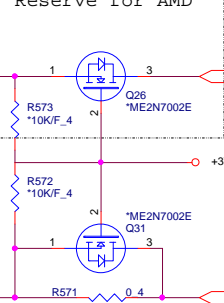


SATA ODD CONNECTOR

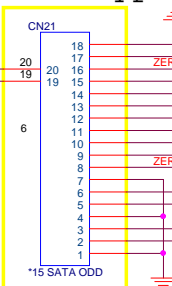
NEW Type Bypass CAP close conn



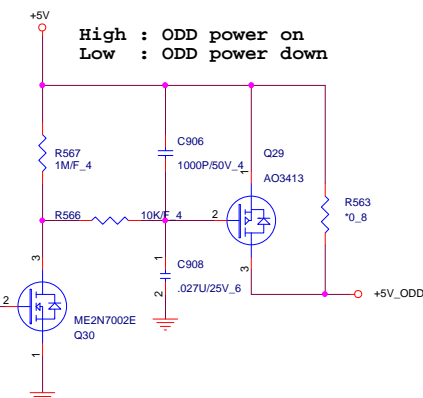
Reserve for AMD



New Type

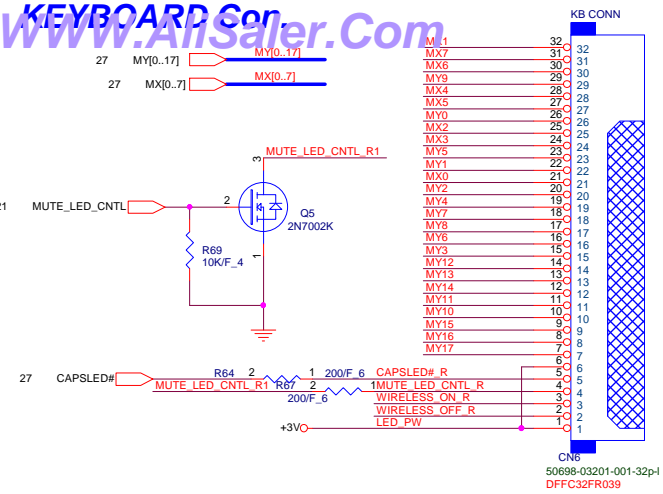


SI Change Footprint



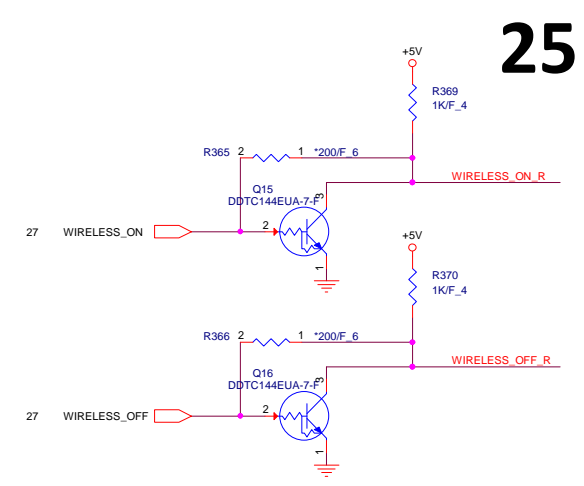
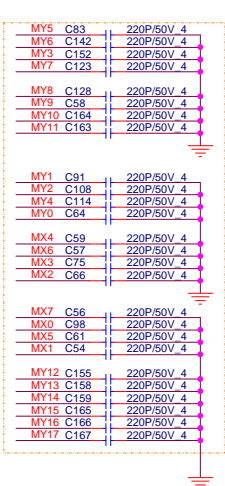
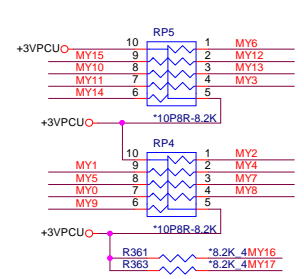
High : ODD power on
Low : ODD power down

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Custom	SATA HDD/ODD/MSATA CONN	1A	
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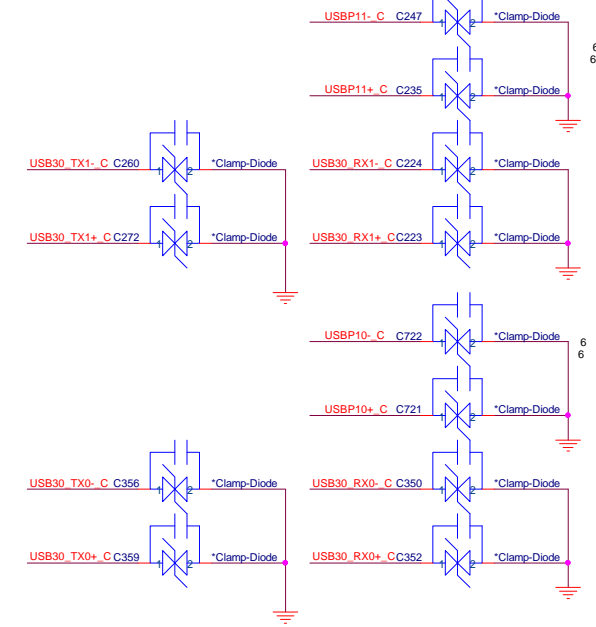


R6X Type

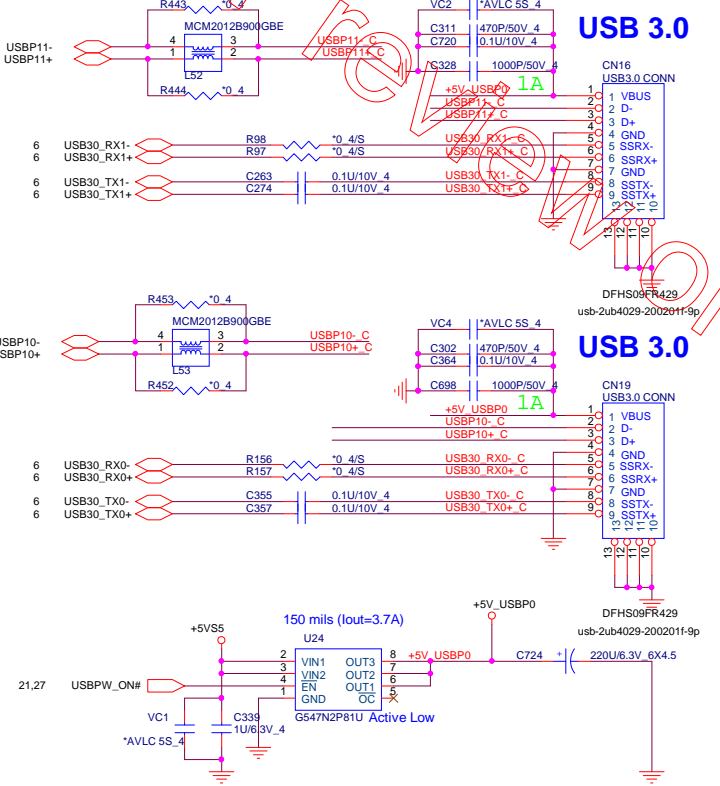
KEYBOARD PULL-UP



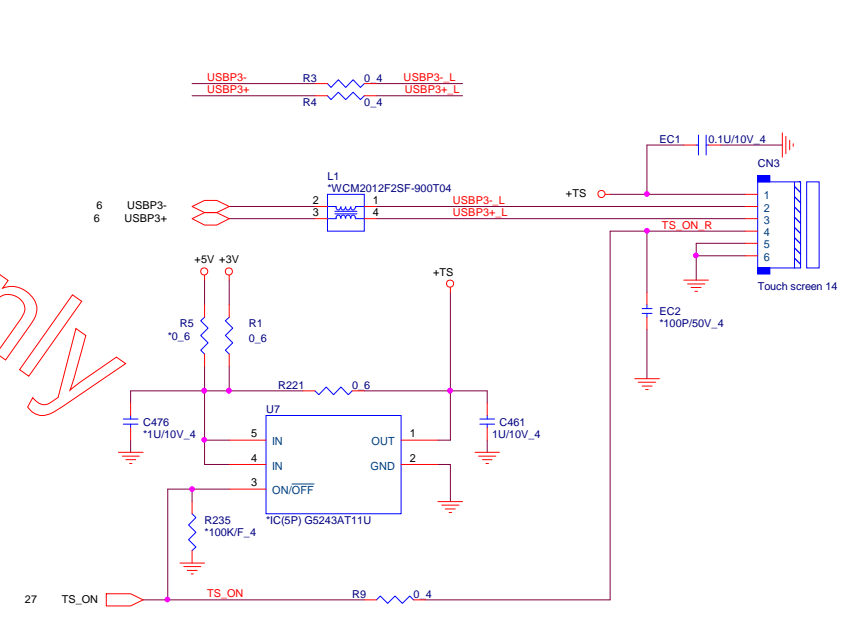
USB 2.0/3.0 Combo




SPS Type



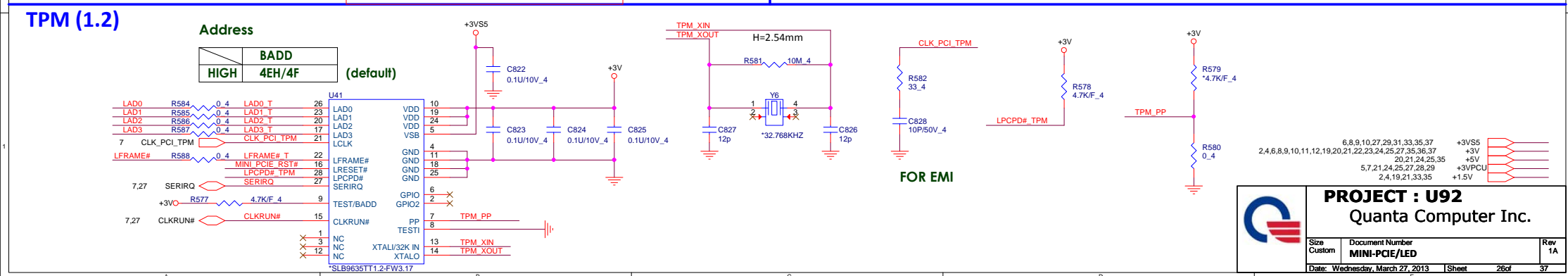
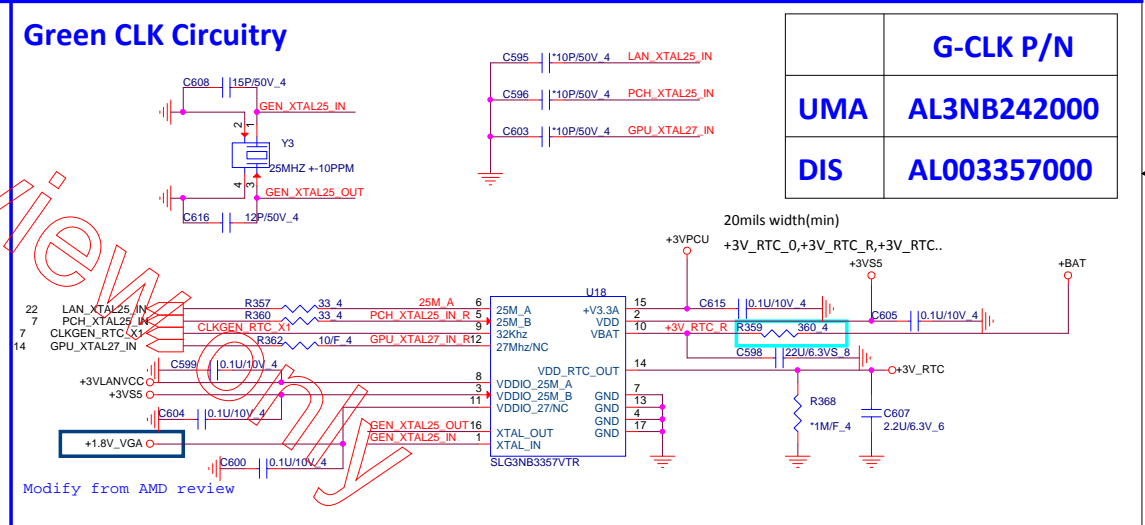
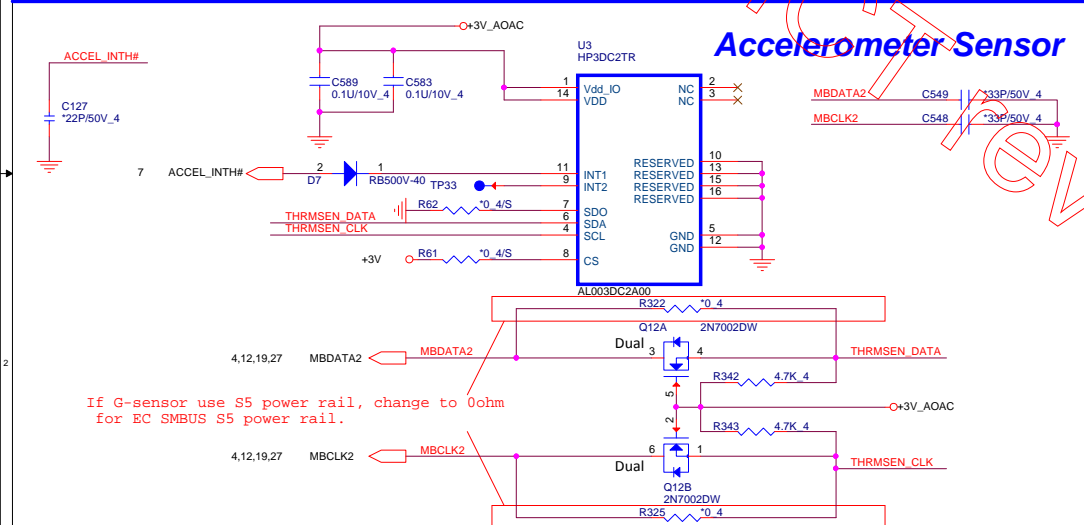
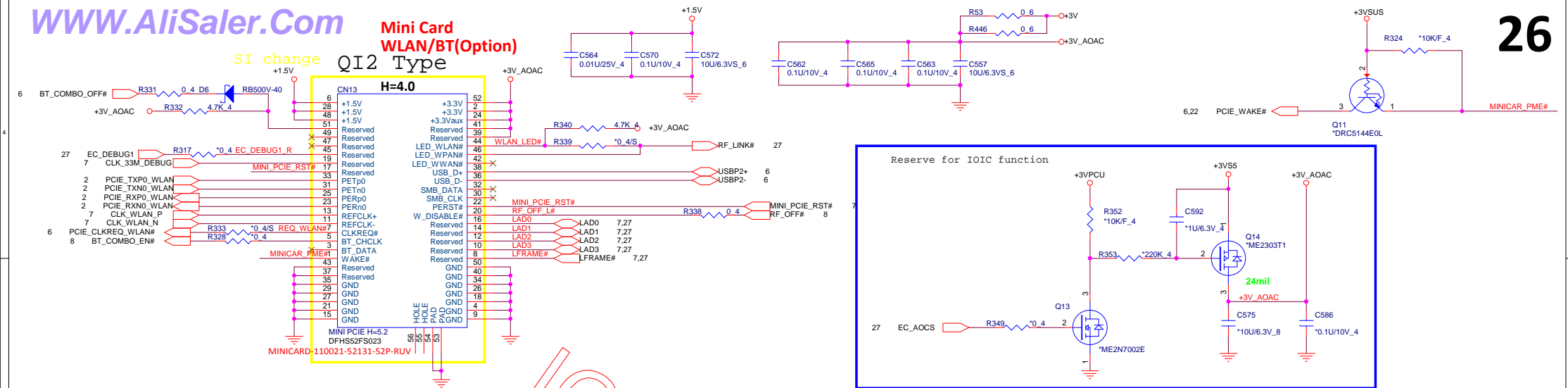
Touch screen



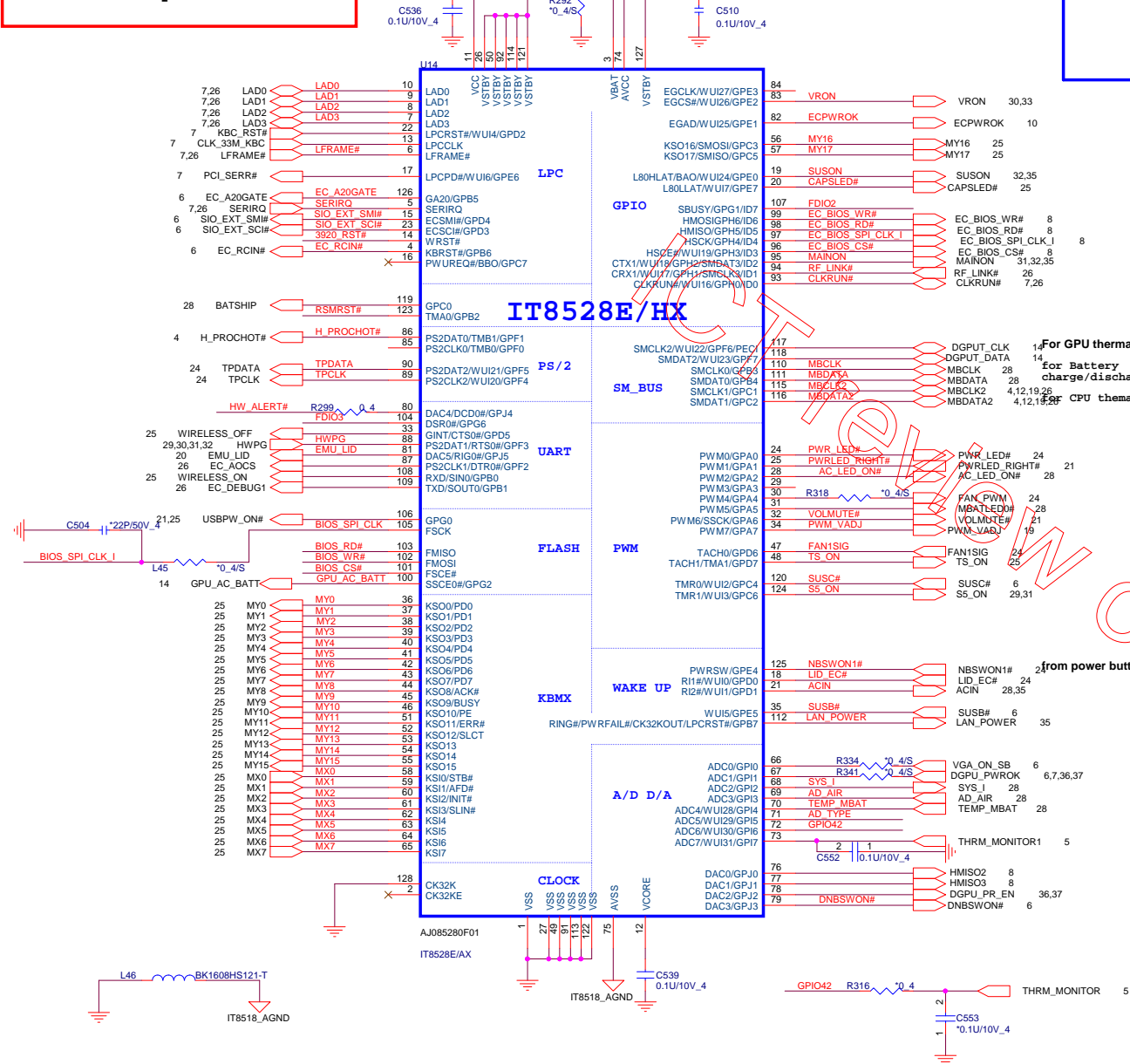


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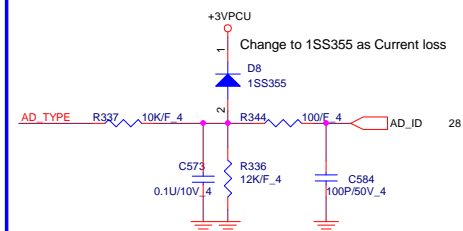
Size	Document Number	Rev
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ITE pin 100 , 104 , 106 default
can not pull up to +3VPCU it
will cause chip into test mode

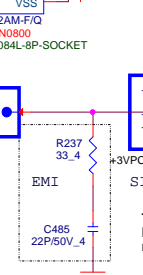
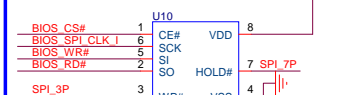


Smart adapter Type check

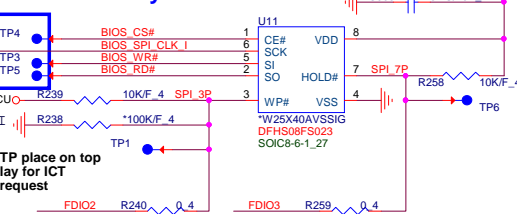


Vender	Size	P/N
AMIC	4M	AKE39F-0800
EON	4M	AKE39ZN0Q02
Socket		DFHS08FS023

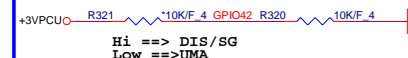
4M SPI EC ROM



128K byte SPI EC ROM



Adapter select



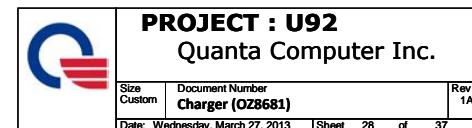
Platform model	GPIO42	adapter
N/A	High	90W
DIS/SG/UMA	Low	65W

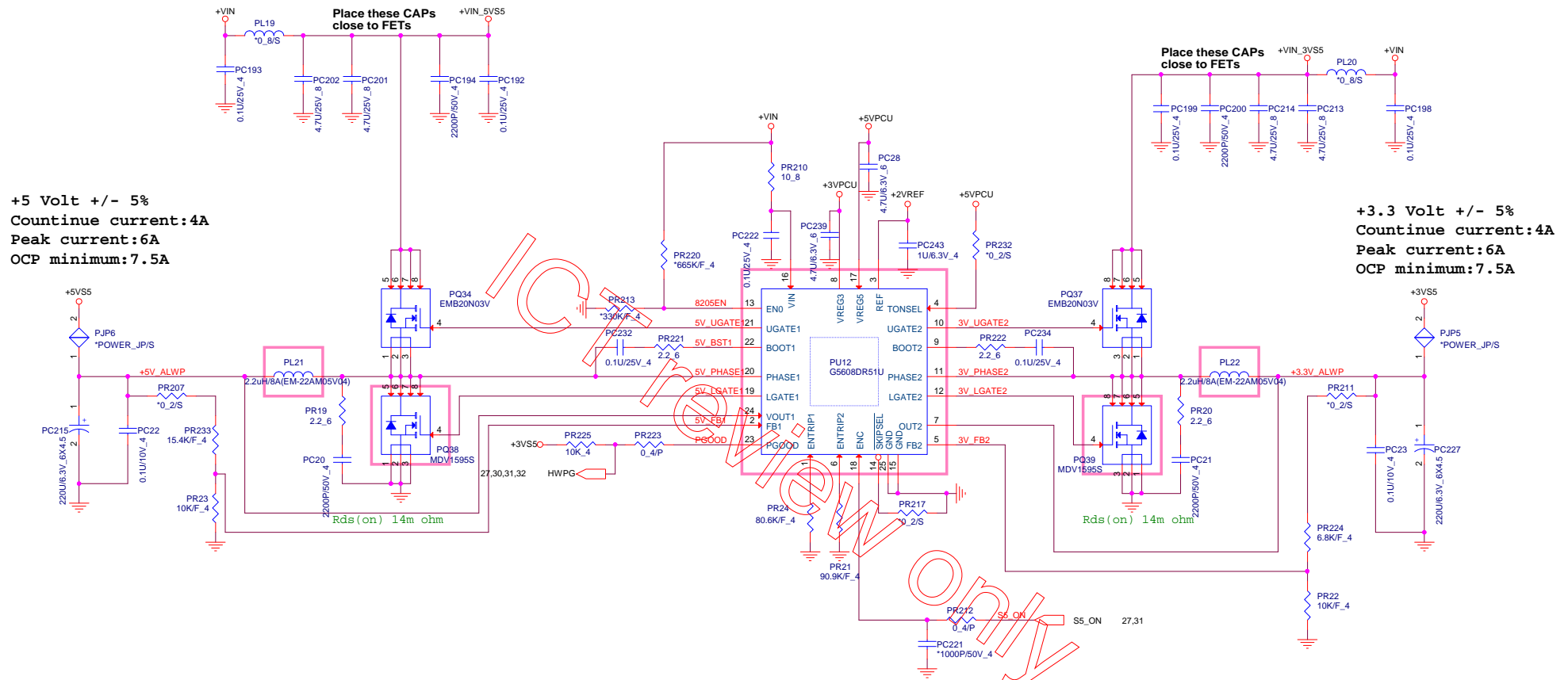
PROJECT : U92
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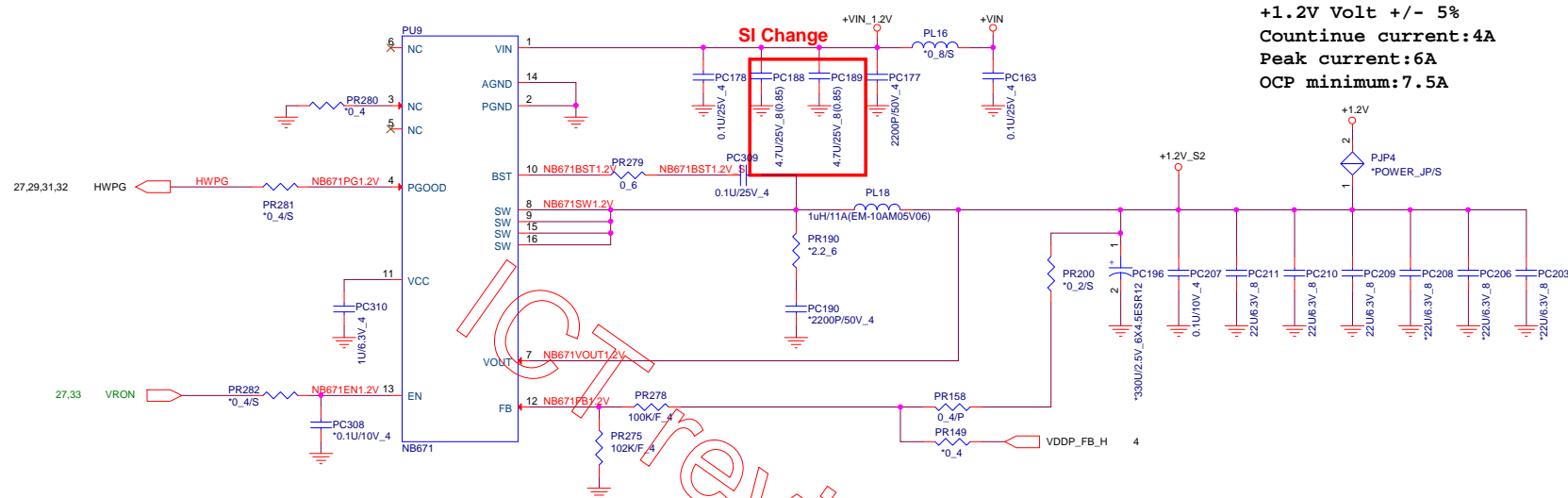



Size Custom	Document Number EC (IT8528E)/ROM	Rev 1
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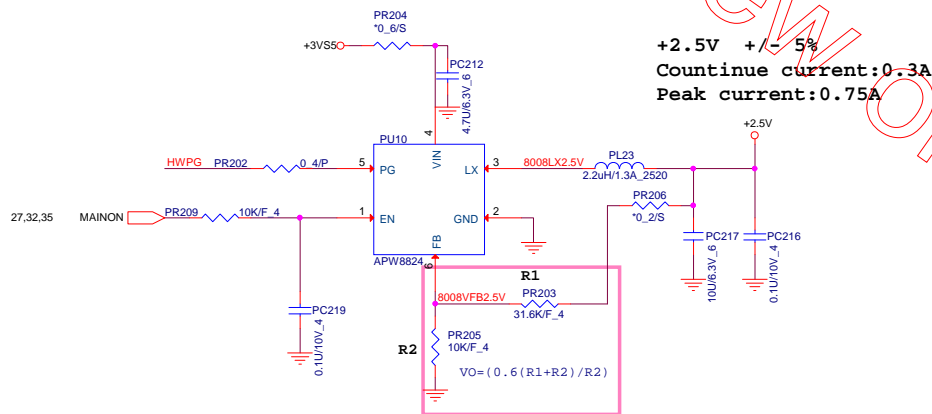
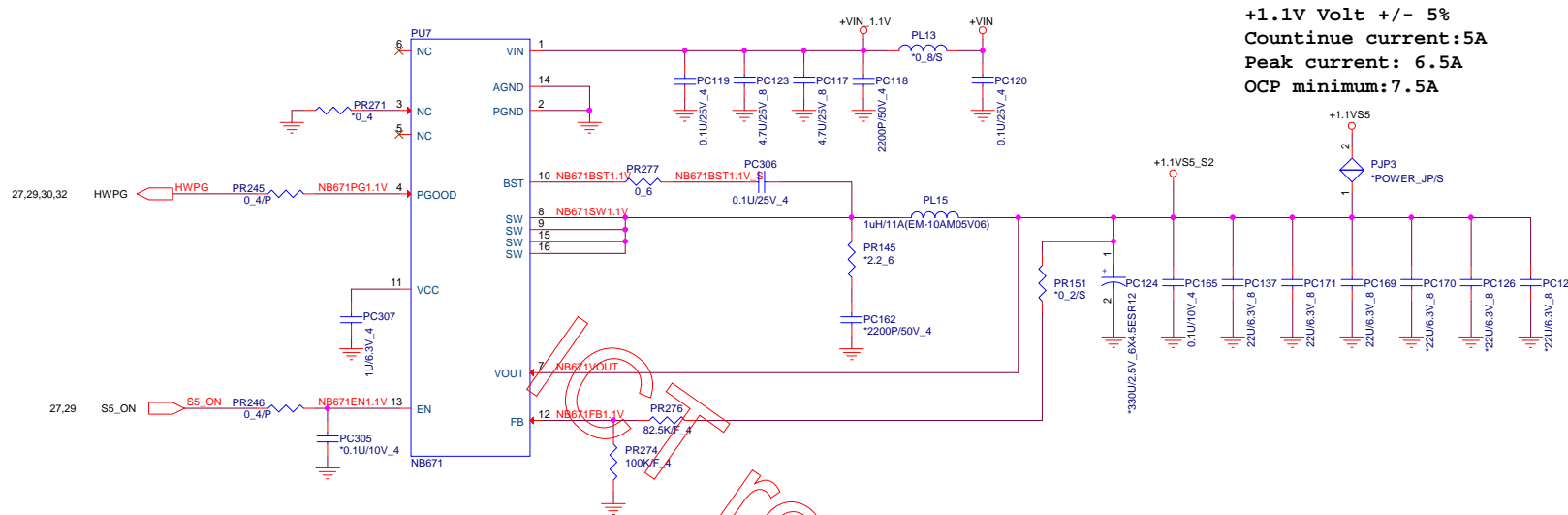
ADD VGA TEMP_FAIL function is active Hi






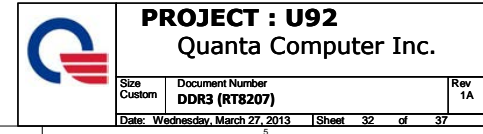


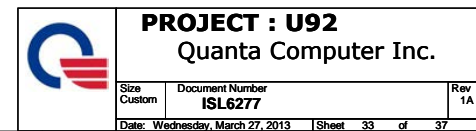
		PROJECT : U92	
		Quanta Computer Inc.	
Size Custom	Document Number +1.2V (RT8228)		Rev 1A
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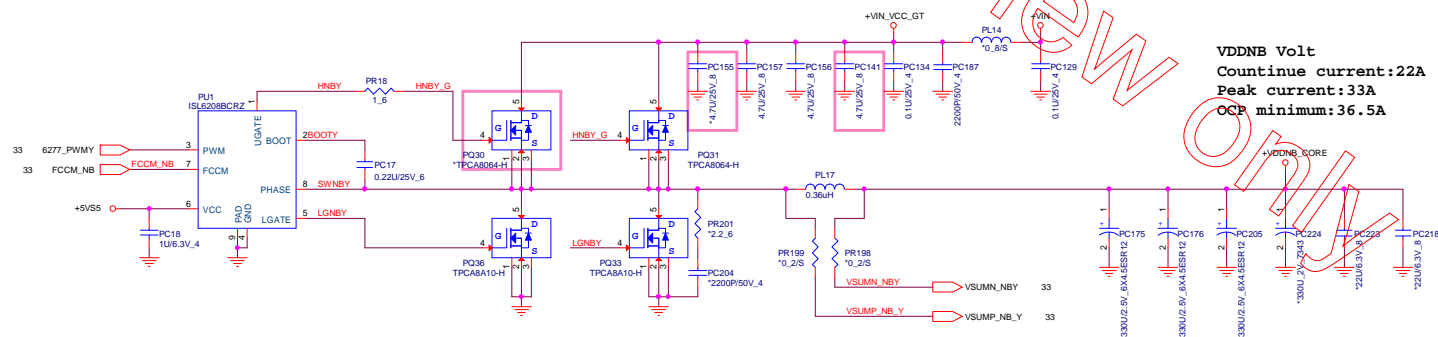
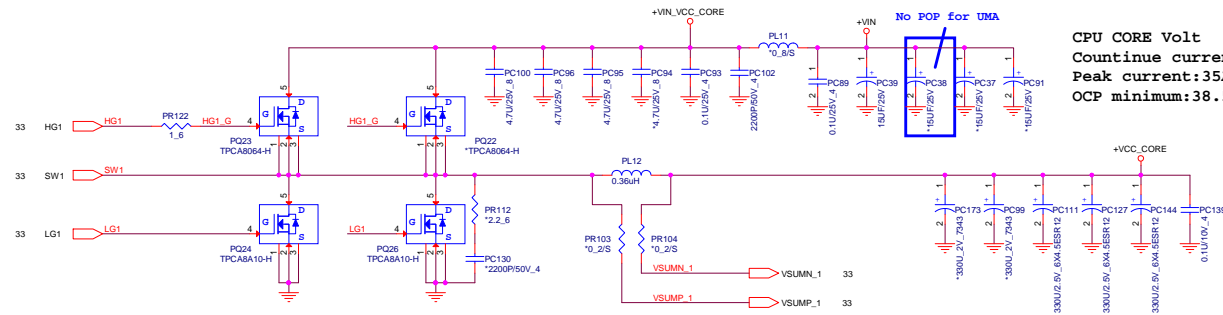


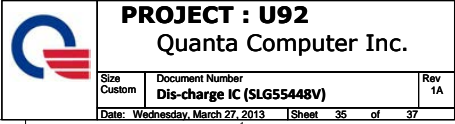
+VIN	20,24,28,29,30,32,34,35,36,37
+2.5V	5
+3VSS	6,8,9,10,26,27,29,33,35,37
+5VSS	21,25,29,32,33,34,35,36,37
+1.1VS5	9,35
+5VPCU	28,29

 PROJECT : U92 Quanta Computer Inc.		
Size Custom	Document Number +1.1VS5 (RT8228)/2.5V	Rev 1A
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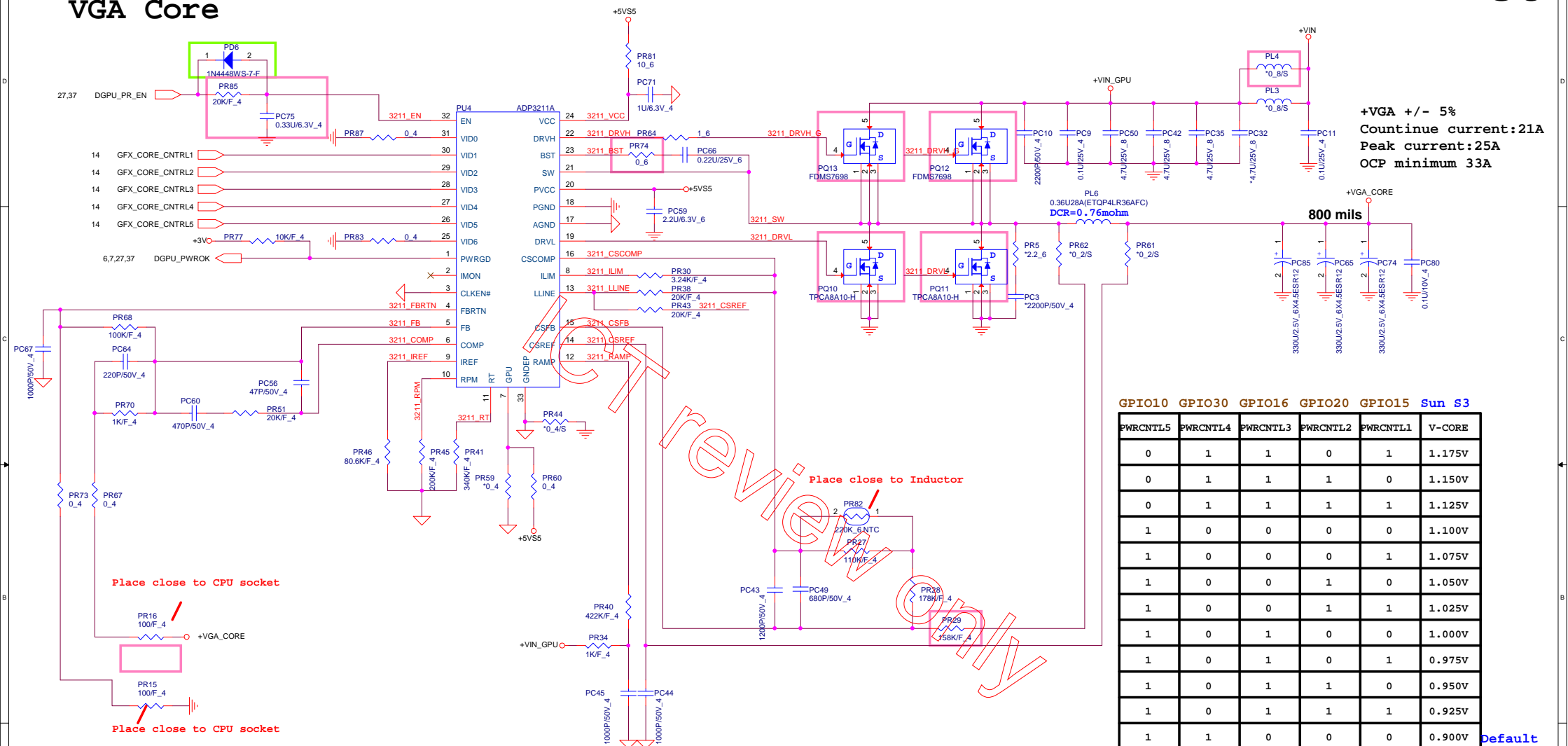






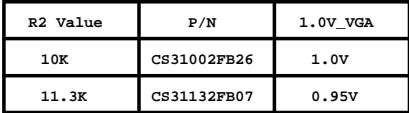


VGA Core



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$$V_0 = 0.6 * (R_1 + R_2) / R_2$$
